IN THE CLAIMS

1-87. (Canceled)

88. (Currently Amended) An integrated circuit structure comprising:

a first substrate comprising a first surface having interconnect contacts; and

a thinned, substantially flexible second substrate comprising a first surface and a second surface ~~each having~~at least one of which has interconnect contacts, wherein the second surface is opposite the first surface and wherein the second surface of the second substrate is polished; and

conductive paths between the interconnect contacts of the first surface of the first substrate and said one of the first surface of the second substrate and the second surface of the second substrate;

wherein the first surface of the first substrate and one of the first surface of the second substrate and the second surface of the second substrate are bonded in a stacked relationship, the first substrate overlapping at least a majority of the second substrate.

89. (Withdrawn) The apparatus of claim 88, wherein the second substrate is one of a thinned monocrystalline semiconductor substrate and a thinned polycrystalline semiconductor substrate.

90. (Withdrawn) The apparatus of claim 88, wherein the circuitry formed on the second substrate is one of active circuitry and passive circuitry.

91. (Withdrawn) The apparatus of claim 88, wherein the circuitry formed on the second substrate consists of both active circuitry and passive circuitry.

92. (Withdrawn) The apparatus of claim 88, wherein the first substrate is a substrate having circuitry formed thereon.

93. (Withdrawn) The apparatus of claim 92, wherein the circuitry of the first substrate is one of active circuitry and passive circuitry.

94. (Withdrawn) The apparatus of claim 92, wherein the circuitry of the first substrate comprises both active circuitry and passive circuitry.

95. (Previously Presented) The structure of claim 88, further comprising:

at least one additional thinned substrate having circuitry formed thereon;

a first of said at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent additional thinned substrate; and

conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between each additional thinned substrate and at least one of said substrates of the integrated circuit structure.

96. (Withdrawn) The apparatus of claim 95, wherein at least two of the first, the second and the at least one additional thinned substrates are formed using a different process technology, wherein the different process technology is selected from the group consisting of DRAM, SRAM, FLASH, EPROM, EEPROM, Ferroelectric and Giant Magneto Resistance.

97. (Withdrawn) The apparatus of claim 95, wherein at least one of the first, the second and the at least one additional thinned substrates comprises a microprocessor.

98. (Withdrawn) The apparatus of claim 95, wherein:

at least one substrate of the first, the second and the at least one additional thinned substrates has memory circuitry formed thereon; and

at least one substrate of the first, the second and the at least one additional thinned substrates has logic circuitry formed thereon that performs tests on the at least one substrate that has memory circuitry formed thereon.

99. (Withdrawn) The apparatus of claim 95, wherein at least one substrate of the first, the second and the at least one additional thinned substrates has

memory circuitry formed thereon, the memory circuitry having a plurality of memory locations, wherein at least one memory location of the plurality of memory locations is used for sparing and wherein data from the at least one memory location on the at least one substrate having memory circuitry formed thereon is used instead of data from a defective memory location on the at least one substrate that has memory circuitry formed thereon.

100. (Withdrawn) The apparatus of claim 95, wherein:

at least one substrate of the first, the second and the at least one additional thinned substrates has memory circuitry formed thereon; and

at least one substrate of the first, the second and the at least one additional thinned substrates has logic circuitry formed thereon that performs programmable gate line address assignment with respect to the at least one substrate having memory circuitry formed thereon.

101. (Withdrawn) The apparatus of claim 95, further comprising a plurality of interior vertical interconnections that traverse at least one of the first, the second and the at least one additional thinned substrates.

102. (Withdrawn) The apparatus of claim 95, wherein information processing is performed on data routed between the circuitry of at least two of the first, the second and the at least one additional thinned substrates.

103. (Withdrawn) The apparatus of claim 95, wherein at least one of the first, the second and the at least one additional thinned substrates has reconfiguration circuitry.

104. (Withdrawn) The apparatus of claim 95, wherein at least one of the first, the second, and the at least one additional thinned substrates has logic circuitry formed thereon for performing at least one function from the group consisting of: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video

encoding, video decoding, voice recognition, handwriting recognition, power management and database processing.

105. (Withdrawn) The apparatus of claim 95, further comprising:

a memory array having a plurality of memory storage cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell stores a data value and has circuitry for coupling the data value to one of the plurality of data lines in response to receiving a gate control signal from one of the plurality of gate lines;

circuitry that generates the gate control signal in response to receiving an address, including means for mapping addresses to gate lines; and

a controller that determines if one of the plurality of memory cells is defective and alters said mapping to remove references to the one of the plurality of memory cells that is defective.

106. (Previously Presented) The structure of claim 95, further comprising:

at least one controller substrate having logic circuitry formed thereon;

at least one memory substrate having memory circuitry formed thereon;

a plurality of data lines and a plurality of gate lines on each memory substrate;

an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines;

a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment; and

controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

107. (Previously Presented) The structure of claim 106, wherein the controller substrate logic:

tests the array of memory cells periodically to determine if one of the array of memory cells is defective; and

removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

108. (Previously Presented) The structure of claim 106, further comprising:

programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

109. (Previously Presented) The structure of claim 106, wherein the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

110. (Previously Presented) The structure of claim 106, wherein:

the logic circuitry of the at least one controller substrate is tested by an external means; and

the array of memory cells of the at least one memory substrate are tested by the logic circuitry of the at least one controller substrate, wherein the testing achieves a functional testing of a substantial portion of the array of memory cells.

111. (Previously Presented) The structure of claim 106, wherein the logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells.

112. (Previously Presented) The structure of claim 106, wherein the controller substrate logic is further configured to:

prevent the use of at least one defective gate line; and

replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

113. (Previously Presented) The structure of claim 106, wherein the controller substrate logic is further configured to prevent the use of at least one defective gate line.

114. (Currently amended) The structure of claim 106, wherein the logic circuitry of the at least one controller substrate can perform all functional testing of the array of memory cells of the at least one memory substrate.

115. (Withdrawn) The apparatus of claim 88, wherein the first substrate is a non-semiconductor material.

116. (Currently Amended) An integrated circuit structure comprising:

a first substrate having topside and bottomside surfaces, wherein the topside surface of the first substrate has interconnect contacts;

a thinned, substantially flexible second substrate having topside and bottomside surfaces, wherein at least one of the topside surface and the bottomside surface of the second substrate ~~have~~ has interconnect contacts, and wherein the bottomside surface of the second substrate is polished;

wherein a major portion of the topside surface of the first substrate and one of the topside surface of the second substrate and the bottomside surface of the second substrate are bonded ~~together~~in a stacked relationship; and

conductive paths between the interconnect contacts on the topside surface of the first substrate and said one of the topside surface of the second substrate and the bottomside surface of the second substrate, the conductive paths providing electrical connections between the first substrate and the second substrate;

wherein the first substrate overlaps at least a majority of the second substrate.

117. (Currently Amended) The integrated circuit structure of claim 116, wherein selected ones of said interconnect contacts of said topside surface of said first

substrate are in electrical contact with selected ones of the interconnect contacts of said bottomside surface of said second substrate so as to form said electrical connections.

118. (Currently Amended) An integrated circuit structure comprising:

a first substrate having a first and second surface;

a second substrate having a first and second surface, wherein said second surfaces of the first and second substrates are opposite to said first surfaces;

wherein at least one of the first substrate and the second substrate is thinned to form at least one thinned, substantially flexible substrate, and wherein the second surface of the at least one thinned, substantially flexible substrate is polished;

wherein the first surface of the first substrate and a major portion of one of the first surface of the second substrate and the second surface of the second substrate are bonded in a stacked relationship by at least one bond, wherein the at least one bond secures a major portion of the second substrate to the first substrate; and

conductive paths between at least two of the first surface of the first substrate and the first and second surfaces of the second substrate, wherein the first substrate overlaps at least a majority of the second substrate.

119. (Previously Presented) The structure of claim 116, further comprising:

at least one additional thinned substrate having circuitry formed thereon;

a first of said at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent additional thinned substrate; and

conductive paths formed between said first of said at least one additional thinned substrate and at least one of said first and second substrates and also between each additional thinned substrate and at least one of said substrates of the integrated circuit structure.

120. (Previously Presented) The structure of claim 119, further comprising:

at least one controller substrate having logic circuitry formed thereon;

at least one memory substrate having memory circuitry formed thereon;

a plurality of data lines and a plurality of gate lines on each memory substrate;

an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines;

a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment; and

controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

121. (Previously Presented) The structure of claim 120, wherein the controller substrate logic:

tests the array of memory cells periodically to determine if one of the array of memory cells is defective; and

removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

122. (Previously Presented) The structure of claim 120, further comprising:

programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

123. (Previously Presented) The structure of claim 120, wherein the array of memory cells are arranged within physical space in a physical order and are

arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

124. (Previously Presented) The structure of claim 120, wherein:

the logic circuitry of the at least one controller substrate is tested by an external means; and

the array of memory cells of the at least one memory substrate are tested by the logic circuitry of the at least one controller substrate, wherein the testing achieves a functional testing of a substantial portion of the array of memory cells.

125. (Previously Presented) The structure of claim 120, wherein the logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells.

126. (Previously Presented) The structure of claim 120, wherein the controller substrate logic is further configured to:

prevent the use of at least one defective gate line; and

replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

127. (Previously Presented) The structure of claim 120, wherein the controller substrate logic is further configured to prevent the use of at least one defective gate line.

128. (Currently amended) The structure of claim 120, wherein the logic circuitry of the at least one controller substrate can perform all functional testing of the array of memory cells of the at least one memory substrate.

129. (Previously presented) The structure of claim 88, wherein the second substrate is thinned to about 50 microns or less.

130. (Previously presented) The structure of claim 116, wherein the second substrate is thinned to about 50 microns or less.

131. (Previously presented) The structure of claim 118, wherein the second substrate is thinned to about 50 microns or less.

132. (Previously presented) The structure of claim 88, wherein the first substrate and the second substrate are the same size or overlap each other completely.

133. (Previously presented) The structure of claim 116, wherein the first substrate and the second substrate are the same size or overlap each other completely.

134. (Previously presented) The structure of claim 118, wherein the first substrate and the second substrate are the same size or overlap each other completely.

135. (New) The structure of claim 88, wherein at least of the first and second substrates comprises a low stress dielectric layer, wherein the low stress dielectric layer is at least one of a silicon dioxide dielectric and an oxide of silicon dielectric and is caused to have a stress of about 5×10^8 dynes/cm^2 or less.

136. (New) The stucture of claim 88, wherein at least of the first and second substrates comprises a low stress dielectric layer, wherein the low stress dielectric layer is at least one of a silicon dioxide dielectric and an oxide of silicon dielectric and is caused to have a stress of about 5×10^8 dynes/cm^2 or less.

137. (New) The structure of claim 116, wherein at least of the first and second substrates comprises a low stress dielectric layer, wherein the low stress dielectric layer is at least one of a silicon dioxide dielectric and an oxide of silicon dielectric and is caused to have a stress of about 5×10^8 dynes/cm^2 or less.

138. (New) The structure of claim 118, further comprising memory circuitry on at least one of the first substrate and the second substrate, wherein a portion of the memory circuit is redundant memory circuitry.

139. (New) The structure of claim 116, further comprising memory circuitry on at least one of the first substrate and the second substrate, wherein a portion of the memory circuit is redundant memory circuitry.

140. (New) The structure of claim 118, further comprising memory circuitry on at least one of the first substrate and the second substrate, wherein a portion of the memory circuit is redundant memory circuitry.